UNIVERSITY of HOUSTON

CULLEN COLLEGE of ENGINEERING Department of Electrical & Computer Engineering

PhD Dissertation Defense Announcement

High-Performance CMOS Front-End ASICs for SiPM Detectors and High-Frequency Ultrasound and Photoacoustic Imaging

Yuxuan Tang

Date: Monday, Dec. 6th, 2021

Time: 12:00 pm to 2:00 pm, CST

Degree: PhD, Electrical Engineering

Location: Zoom

https://uh-edu-cougarnet.zoom.us/j/95718125871?pwd=Ry9LQ3dMZWpnS0dqVnR3ZnhtbWR2dz09

Committee Chair: Dr. Jinghong Chen

Committee Members: Dr. Wanda Wosik Dr. Yuhua Chen Dr. Xin Fu Dr. Jiming Peng Dr. David Jackson

Abstract:

Silicon photomultiplier (SiPM), as a high sensitivity photon detector, has been widely used in high energy physics, positron emission tomography imaging, and light detection and ranging applications. The slow-rising edge of the standard SiPM signal, however, makes the timing measurement sensitive to noise and leads to poor timing resolution performance. Besides, the SiPM energy measurement utilizing charge-sensitive amplifiers (CSAs) suffers from high power consumption and thus is not suitable for applications with a large number of SiPM detectors. To solve these issues, two hardware prototypes in a 180 nm CMOS process have been fabricated and experimentally characterized. The first prototype is a single-channel SiPM readout featuring an on-chip fast signal generator and a customized successive-approximation-register (SAR) analog-to-digital converter (ADC). The on-chip fast-signal generator sharpens the slow-rising edge of the SiPM charge integrator as the ADC track-and-hold circuit,

lowering the ADC power consumption. Measurement results show the readout front-end achieves a gain non-linearity of 3.3% over 800 pC input charge range, a timing resolution of 151 ps, while dissipating 4.02 mW of power. The second prototype demonstrates a shared SAR ADC architecture in multi-channel SiPM readout to reduce the chip area and power consumption and a highly-linear FPGA-based time-to-digital converter (TDC). The ADC is shared by 16 readout channels in a time-multiplexed manner and achieves an SFDR of 58.34 dB and an SNDR of 51.37 dB at 16 MS/s. Implemented in a Xilinx 28 nm Kintex-7 FPGA, the FPGA-based TDC achieves a 15 ps root mean square resolution, a differential nonlinearity of 4 ps, and an integral nonlinearity of less than 10 ps.

High-frequency (30~100 MHz) ultrasound and photoacoustic imaging with improved microscopic resolution opens new medical applications in the fields of ophthalmology, dermatology, intravascular imaging and systemic sclerosis. To break the tradeoff between noise and wideband impedance matching, the second part of the dissertation develops a wideband low-noise amplifier (LNA) front-end with noise and distortion cancellation. The LNA employs a resistive shunt-feedback structure with a feedforward noise-canceling technique to accomplish both wideband impedance matching and low-noise performance. A complementary CMOS topology is also developed to cancel the second-order harmonic distortion and enhance the amplifier linearity. A high-frequency ultrasound and photoacoustic imaging front-end including the proposed LNA and a variable gain amplifier is designed and fabricated in a 180 nm CMOS process. At 80 MHz, the front-end achieves an input-referred noise density of 1.36 nV/sqrt(Hz), an input return loss of better than -16 dB, a voltage gain of 37 dB, and a total harmonic distortion of -55 dBc while dissipating a power of 37 mW, leading to a noise efficiency factor of 2.66.