Defense Announcement

Network Attached Hardware Block (NAHB) Framework

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Modern FPGA (Field Programmable Gate Array) systems have significant data processing capabilities but limited memory and storage capabilities. This thesis creates a common framework by which multiple logic modules within one or more FPGAs may offload data to and access data from connected resources such as a server or other FPGA/SOC system on a network. This implementation, which will be called the Network Attached Block (NAHB) framework is entirely hardware based and maintains high throughput and low latency without a software/firmware network stack. The proposed protocol may be utilized across a variety of physical layer types, but will be designed to function on a Gigabit Ethernet network as an example.

Such a common framework allows for robust and simplified development of multi-FPGA systems that can take advantage of direct connected or network connected resources. This framework shares a network connection between multiple endpoints within a device and will allow for arbitration between endpoints.