High resolution multi-level voltage space vector structure generation for variable speed drives and grid-tied applications

Prof. K. Gopakumar
DESE, Indian Institute of Science

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LECTURE ABSTRACT

Recently, numerous interesting multilevel topologies have been reported for motor drive applications. However, to date, the most popular topology is the neutral point clamped (NPC) three-level topology. Especially for medium-voltage drives applications. This shows that the industry is still looking for viable alternative to this topology, with reduced power circuit complexity and increased reliability for medium-voltage drives applications. This specific lecture will focus on some of the recent work from my lab on five-level , nine-level inverter topologies and 17-level multilevel topologies, with reduced DC-link voltages, enabling multilevel back- to- back inverter operation for medium voltage drives. This is followed by some recent work on multilevel topologies, with stacked low voltage inverter cells, polygonal voltage space vector generation with dodecagonal, octadecagonal and 24-sided structures for variable speed drives.

SPEAKER BIOSKETCH

Dr. K. Gopakumar (M'94-SM'96-F'11) received his B.E., M.Sc. (Engg.), and Ph.D. degrees in Electrical Engineering from the Indian Institute of Science, Bangalore, India, in 1980, 1984, and 1994, respectively. He was with the Indian Space Research Organization, Bangalore, India from 1984 to 1987. He currently holds the position of Professor at the Department of Electronics System Engineering, Indian Institute of Science. Dr. Gopakumar is a Fellow of IEEE, IETE India and INAE. He is currently a Co-Editor in Chief of IEEE Transactions on Industrial Electronics. He was also a Distinguished Lecturer of IEEE Industrial Electronics Society (IES) from 2012 to 2017. His research interests include PWM converters and high power drives.